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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,478	08/22/2003	Daisuke Kawagoe	884.937US1	9311

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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,478	KAWAGOE, DAISUKE	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *attachment "A"*.

DETAILED ACTION

1. This action is in response to amendment filed on April 14, 2005.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first skip via is in a cylindrical shape, as claimed in claim 29 and 38, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 22-39 are objected to because of the following:

Regarding claim 22: The language "the first conductive layer including a first skip via extending through the first dielectric layer and a third dielectric layer" and "the second conductive layer, including a second via extending through the second dielectric layer", is not clear. The relationship of skip via or second via with first and conductive layer and the second conductive layer and their respective positions are not clear. For the examination purpose the considered the skip via in contact with the first conductive layer and the second via is in contact with the second conductive layer.

Claims 23-30 directly depend from claim 22 and inherit the same deficiency.

Regarding claim 31, The language "the first conductive layer including a first skip via extending through the first dielectric layer and a third dielectric layer" and "the second conductive layer, including a second skip via extending through the second dielectric layer and fourth dielectric layer", is not clear. The relationship of first skip via or second skip via with first conductive layer and the second conductive layer and their respective positions are not clear. For the examination purpose the considered the first skip via in contact with the first conductive layer and the second skip via is in contact with the second conductive layer.

Claims 32-39 directly depend from claim 31 and inherit the same deficiency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 22-25 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter et al., US Patent No., 6,810,583.

Regarding claim 22, Carpenter et al., in an embodiment of figure 6, discloses a substrate comprising: a first conductive layer (14) between a first dielectric layer (41) and a second dielectric layer (15), the first conductive layer including a first skip via (56) extending through the first dielectric layer (41) and a third dielectric layer (43); and a second conductive layer (116) on the second dielectric layer (15), the second conductive layer, including a second via (24) extending through the second dielectric layer, the second via (24) and the first skip via (56) being stacked on top of one another (see figure 6).

Regarding claim 23, Carpenter et al., further discloses first skip via includes a longitudinal axis (longitudinal axis passing through via 56) and the second via includes a longitudinal axis (longitudinal axis passing through via 24), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via (see figure 6).

Regarding claim 24, Carpenter et al., further discloses first, second and third dielectric layers (41, 15 and 43) are formed on a core (143) and the first (14) and second conductive layers (116) are formed on the core (143).

Regarding claim 25, Carpenter et al., further discloses the second conductive layer is between the second dielectric layer (13) and a fourth dielectric layer (141).

Regarding claim 28, Carpenter et al., further discloses the first conductive layer (14) is a patterned conductive layer and the second conductive layer (116) is a patterned conductive layer.

6. Claims 31-34 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter et al., US Patent No., 6,810,583.

Regarding claim 31, Carpenter et al., in another embodiment of figure 7, (figure 7 with marked elements as shown in attachment "A"), discloses a substrate comprising:

a first conductive layer (C3) between a first dielectric layer (D2) and a second dielectric layer (D3), the first conductive layer including a first skip via (V1) extending through the first dielectric layer (D2) and a third dielectric layer (D1); and a second conductive layer on a fourth dielectric layer (D4), the second conductive layer including a second skip via (V2) extending through the second dielectric layer and the fourth dielectric layer (D4), the first skip via and the second skip via being stacked on top of one another (see figure 7, appendix A).

Regarding claim 32, Carpenter et al., further discloses the first skip via (V1) includes a longitudinal axis (longitudinal axis passing through via V1) and the second skip via (V2) includes a longitudinal axis (longitudinal axis passing through via V2), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via (see figure 7, appendix A).

Regarding claim 33, Carpenter et al., further discloses the first (D2), second (D3), third (D1) and fourth (D4) dielectric layers are formed on a core (D6) and the first (C3) and second conductive layers (C5) are formed on the core (D6).

Regarding claim 34, Carpenter et al., further discloses the second conductive layer (C5) is between the fourth dielectric layer (D4) and a fifth dielectric layer (D5).

Regarding claim 37, Carpenter et al., further discloses the first conductive layer is a patterned conductive layer and the second conductive layer is a patterned conductive layer (see figure 7, appendix "A").

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., US Patent No., 6,810,583.

Regarding claim 26, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 25 above, in the embodiment of figure 6, including a third conductive layer (142) on the fourth dielectric layer (141), a third via (156) extending through the fourth dielectric layer, the third via being stacked onto the first skip via and the second via (see figure 6).

Carpenter et al., does not disclose the conductive layer connected to third via (156). However, as can be seen at various places in the figure, the conductor layer / patterns are connected to the via depending upon the desired electrical connections for signal, power and ground.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with the

third via connected to the third conductive layer, in order to have desired electrical connection for signal, power or ground.

Regarding claim 27, Carpenter et al., further discloses the first skip via (56) includes a longitudinal axis (axis passing longitudinally through the via) and the second (24) and third (156) vias each include a longitudinal axis (axis passing longitudinally through the vias), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via and the longitudinal axis of the third via (see figure 6.

9. Claims 35 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., US Patent No., 6,810,583.

Regarding claim 35, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 35 above, the embodiment of figure 7 (elements marked on figure 7 in attachment "A"), including a third conductive layer (C6) on the fifth dielectric layer (D5), a third via (V3) extending through the fifth dielectric layer, the third via (V3) being stacked onto the first skip via (V1) and the second skip via (V2).

Carpenter et al., does not disclose the conductive layer connected to third via (V3). However, as can be seen at various places in the figure, the conductor layer / patterns are connected to the via depending upon the desired electrical connections for signal, power and ground.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with the third via connected to the third conductive layer, in order to have desired electrical connection for signal, power or ground.

Regarding claim 36, Carpenter et al., further discloses the first (V1) and second (V2) skip vias each include a longitudinal axis (axis passing longitudinally through the vias) and the third via includes a longitudinal axis (axis passing longitudinally through the via), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via and the longitudinal axis of the third via (see figure 7, appendix "A).

10. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., as applied to claim 22 above, and further in view of Uchikawa et al., US Patent No. 6,531,661, Asai et al., US Patent No. 6,534,723 and Kumar, US Patent No. 5,227,013.

Regarding claim 29, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 22 above, in the embodiment of figure 6, including the second via (24) as cylindrical via, but does not disclose the first skip via as a cylindrical via. Also, Carpenter et al., is silent about the diameters of both the vias. However, as can be seen from figure 6, both cylindrical and tapered via holes are known in the art. Also, cylindrical via holes made using drilling method are well known in the art.

A person of ordinary skill in the art would decide the shape of the via based on the method of manufacturing the via and also on the method of filling the conductive via to make them conductive.

Uchikawa et al., discloses via hole made by drilling, laser beam application, plasma etching or photography to have an inner diameter of 30 to 200 μm (column 3, line 33-35).

Asai et al., discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Kumar, in figure 6, discloses a multilayer circuit board with cylindrical holes traveling to more than two layers.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., the first skip via in a cylindrical shape, in order to form the via by well known drilling method and to have the via diameters of both the vias as claimed, in order to facilitate filling of conductive material to have reliable electrical connection, as disclosed by Uchikawa et al., and Asai et al and Kumar.

Regarding claim 30, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 22 above, in the embodiment of figure 6, but does not disclose the length of first skip via between 58 μm and 85 μm and that of second via

between 24 μm and 36 μm. However the length of the via will depend upon the thicknesses of the insulating layers of the circuit board and the number of the insulating board layer the via travels. As applied to claim 29, Asai et al., discloses insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance. Also, Kumar discloses cylindrical skip vias traveling more than two layers.

Therefore, it would have been obvious to person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with via lengths of both the vias as claimed, in order to have electrical connection between the different layer of the circuit board, which can have thicknesses from 20 to 600 μm to assure a sufficient insulation performance, as taught by Asai et al. and Kumar.

11. Claims 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., as applied to claim 31 above, and further in view of Uchikawa et al., US Patent No. 6,531,661, Asai et al., US Patent No. 6,534,723 and Kumar, US Patent No. 5,227,013.

Regarding claim 38, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 31 above, in the embodiment of figure 7 (with the elements as marked on figure 7 in attachment "A") including the second skip via (V2) as a cylindrical via, but does not disclose the first skip via as a cylindrical via. Also, Carpenter et al., is silent about the diameters of both the vias. However, as can be seen

from figure 7, both cylindrical and tapered via holes are known in the art. Also, cylindrical via holes made using drilling method are well known in the art.

A person of ordinary skill in the art would decide the shape of the via based on the method of manufacturing the via and also on the method of filling the conductive via to them make them conductive.

Uchikawa et al., discloses via hole made by drilling, laser beam application, plasma etching or photography to have an inner diameter of 30 to 200 μm (column 3, line 33-35).

Asai et al., discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm, to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Kumar, in figure 6, discloses a multilayer circuit board with cylindrical holes traveling to more than two layers.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., the first skip via in a cylindrical shape, in order to form the via by well known drilling method and to have the via diameters for both the vias as claimed, in order to facilitate filling of conductive material to have reliable electrical connection, as disclosed by Uchikawa et al., and Asai et al.

Regarding claim 30, Carpenter et al., discloses all the features of the claimed invention, as applied to claim 31 above, in the embodiment of figure 7 (with the elements as marked on figure 7 in attachment "A"), but does not disclose the length of first skip via between 58 μm and 85 μm and that of second skip via between 24 μm and 36 μm. However the length of the via will depend upon the thicknesses of the insulating layers of the circuit board and the number of the insulating board layer the via travels. As applied to claim 29, Asai et al., discloses insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance. Also, Kumar discloses cylindrical skip vias traveling more than two layers.

Therefore, it would have been obvious to person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with via lengths of both vias as claimed, in order to have electrical connection between the different layer of the circuit board, which can have thicknesses from 20 to 600 μm to assure a sufficient insulation performance, as taught by Asai et al., and Kumar.

Response to Arguments

12. Applicant's arguments with respect to claims 22-39 have been considered but are moot in view of the new ground(s) / new explanation of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Burgess, US Patent Application Publication No. 2001/0020548, in figure (26) discloses a circuit board with skip via.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IB
June 23, 2005.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Attachment 'A'

application # 10/646,478
GAU : 2841

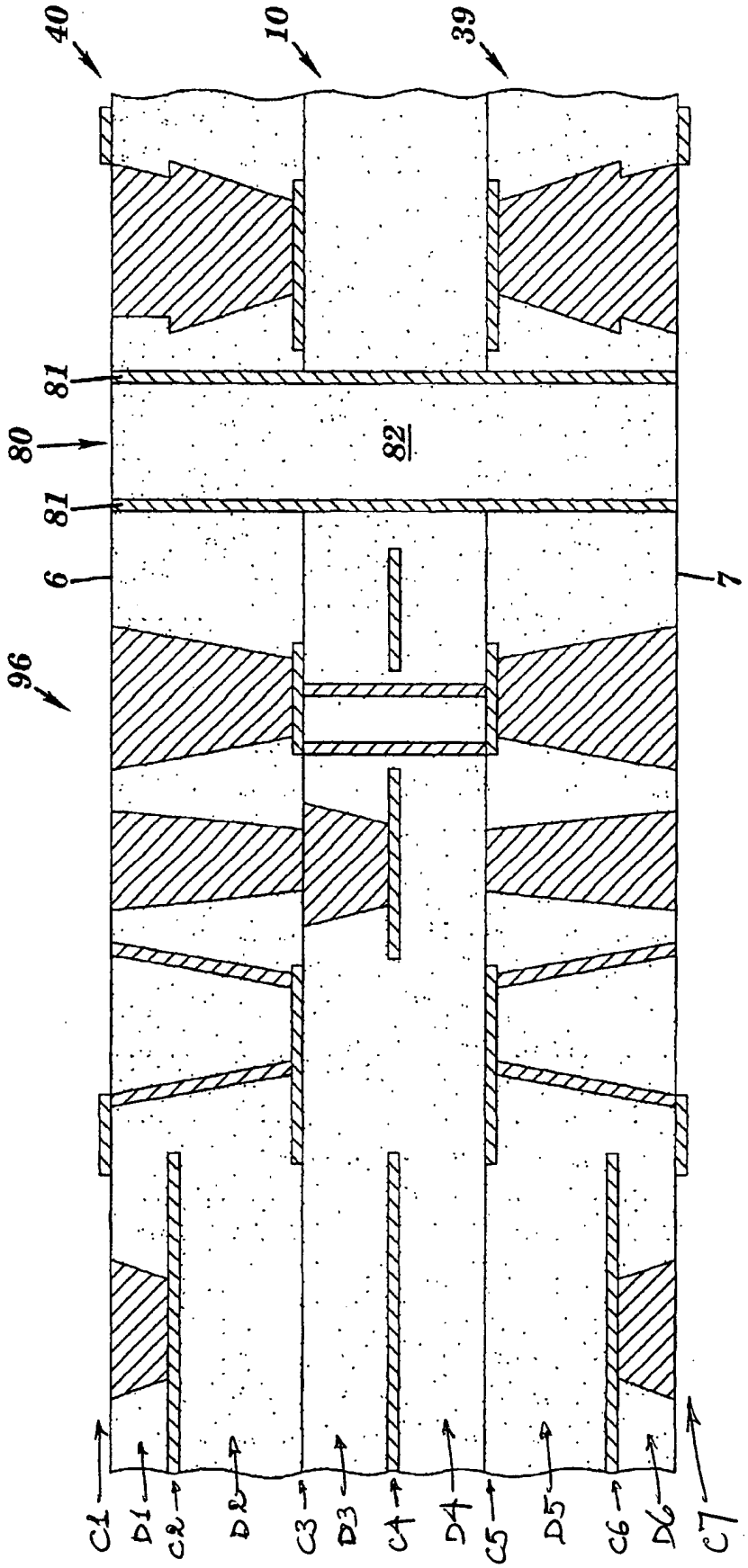

FIG. 7

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